SURANJANA VERMA
M.Tech (VLSI), B.Tech (E&TC Engg.)

Recent Address: Flat No-B3-603
Building No-B3, 6th Floor, Nyati Evara Sociey,
Mohammed wadi,Undri, Pune-411060

Permanent Address: Soudamini Nivas,
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Markat Nagar, Near Amar Palace
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OBJECTIVE

To work with integrity as a team member, in a reputed organization and play an active role in its growth and development and in turn learn and improve personally from my experience.

PROFESSIONAL QUALIFICATION

Post-Graduation :M.Tech (VLSI Design) (2010 – 2012) from Dr M.G.R Educational and Research Institute University, Chennai
Marks Scored : 8.95/10 CGPA
Graduation : B.Tech (Electronics & Telecommunication Engg.) (2006-2010) from Synergy Institute of Engineering and Technology, Dhenkanal under BPUT (Biju Pattnaik University of Technology), Rourkela
Marks scored : 7.69/10 CGPA

SKILL SUMMARY

Languages : VHDL, C
Tools : Mentor Graphics –> Modelsim
XILINX
Operating Systems: All editions of Windows.

AREAS OF INTEREST

I. Digital Logic Design.
II. Digital Design Verification.

EXPERIENCE IN CHRONOLOGICAL ORDER.

I. DESIGNATION:- **Content Developer (Translator and proof reader)**
COMPANY: - **Mulltibhashi Solutions Private Limited**
PERIOD: - **July, 2020 – Till Date (Work from home.)**

II. DESIGNATION:- **Oriya Translator**
COMPANY: - **Galama Multilingual Translation Company**
PERIOD: - **February, 2021 – Till Date (Work from home.)**

III. DESIGNATION:- **Content Auditor**
COMPANY: - **Gig India**
PERIOD: - **April,2019 – October,2019(Work from home.)**

IV. DESIGNATION:- **Tele-calling Execuive**
COMPANY: - **Squadrun Application, New Delhi**
PERIOD: - **March, 2018 – October,2019(Work from home.)**

V. DESIGNATION:- **Assistant Professor**
COLLEGE: - **G H Raisoni College of Engineering & Management,Pune**
PERIOD: - **October, 2016 – July, 2017**

VI. DESIGNATION:- **Assistant Professor**
COLLEGE:-**C.V.RamanCollege Of Engineering, Bhubaneswar**
PERIOD: - **January, 2013 – July, 2016**

VII. DESIGNATION:- **Technical Associate (Non- voice)**
COMPANY: - **Sify Technologies, Chennai**
PERIOD: - **Jan 2012 – Sep 2012**

PROJECTS COMPLETED

I. ASIC Based Hardware Architecture for System Protection against Multiple Concurrent Threats. (M.Tech)
II. Car Security System (BE)

ACADEMIC ROLE

I. Served as scrutinizer, question setter and examiner for the autonomous batches.

II. Assigned with teaching of various UG & PG subjects like Microprocessor, Digital Electronics Circuit, Basic Electronics and Microprocessor & Assembly Language Programming respectively.

III. Involved in proctoring system of UG students.

IV. Guided 4 nos. of B.Tech project groups.

V. Seminar Coordinator for B. Tech Students for the year 2015.

VI. Coordinator for Final Year Students of 2011-2015 batch B. Tech students.

VII. Activity Co-Ordinator for B. Tech Students for the year 2017.

CO-CURRICULAR ACTIVITIES

I. One of active Committee member of International Conference on "Signal processing, Computing and Networking" 2017.

II. One of active Organizer of International Conference on "Man and Machine Interfacing MAMI-2015", Technical Co-Sponsor By IEEE Kolkata Section.

III. Appreciated by Texas Instruments India for Mentoring a Project in "Texas Instruments Innovation Challenge India Design contest 2015".

IV. Organizer and participant of National Conference on "VlSI Signal Processing and Trends in Telecommunication VS@TT'13" at C V Raman College of Engg. ,BBSR.

V. Organizer and participant of National Conference on "VlSI Signal Processing and Trends in Telecommunication VS@TT'14" at C V Raman College of Engg. ,BBSR.

VI. Participant of AICTE Sponsored Faculty Development Programme on "Selected Topics in VLSI Design & Embedded System (STVDES 2015)" at C V Raman College of Engg. BBSR.

VII. Presented a Paper on "High performance Parallel Interface on National Conference about Applications Of Analog and Digital Devices" at Dr. M G R University, Chennai.

VIII. Participated in 9th Annual State level Students Convention of ISTE(Indian Society for Technical Education) Odisha at Synergy Institute of Engg. & Tech.

EXTRA CURRICULAR ACTIVITIES

I. Member of the organizing committee for the farewell functions conducted by 3rd Year batch in C V Raman College of Engg.

II. One of the members of the organizing committee for the cultural function CELEGANCE 2013, 2014, 2015 conducted by C V Raman College of Engg.

PERSONAL DETAILS

Date of Birth	: 17th July 1988
Father's Name	: Mr. Debabrata Verma
Mother's Name	: Mrs. Nibedita Verma
Nationality	: Indian
Gender	: Female
Marital Status	: Married

Languages Known : English, Hindi, Odia.
Hobbies : Playing volley ball, Listening to music, Dancing

DECLARATION

I declare that the above information furnished is true to the best of my knowledge.

Date:
Place: (Suranjana Verma)